Power Delivery Network (PDN) Analysis

Edoardo Genovese
Importance of PDN Design

Power Deliver Network (PDN)

- Ensure clean power
- Signal Integrity
- EMC Limit
Power Delivery Network (PDN)

PDN consists:
1. VRM (voltage regulator module)
2. Capacitors (Decoupling/Bypass)
3. PCB parasitic impedance
4. Active device (On Package Decap)
Power Integrity Simulation

- IR-Drop
- AC PI Analysis
  - Decap Analysis Tool
- SSO from DDR2 Module
  - PCB+Pckg+Chip
Board Description

- 8 metal layers board with total thickness 1.696mm
- 1.8V power plane to be analyzed located in 4th layer
- 1 memory controller and 2 DDR2 memory modules
## IR-Drop Simulation

<table>
<thead>
<tr>
<th>Component</th>
<th>Voltage (V)</th>
<th>VDD Drop (V)</th>
<th>GND Drop (V)</th>
<th>DC Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory controller Group</td>
<td>1.78849</td>
<td>10.507m</td>
<td>1.007m</td>
<td>575mOhm</td>
</tr>
<tr>
<td>Memory Module I Group</td>
<td>1.7889</td>
<td>10m</td>
<td>0.969m</td>
<td>498mOhm</td>
</tr>
<tr>
<td>Memory Module II Group</td>
<td>1.789</td>
<td>9.409m</td>
<td>0.929m</td>
<td>469mOhm</td>
</tr>
</tbody>
</table>

### JEDEC 79-2F

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Rating</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply Voltage</td>
<td>1.7</td>
<td>1.8</td>
<td>1.9</td>
<td></td>
</tr>
<tr>
<td>VDDL</td>
<td>Supply Voltage for DLL</td>
<td>1.7</td>
<td>1.8</td>
<td>1.9</td>
<td></td>
</tr>
<tr>
<td>VDDQ</td>
<td>Supply Voltage for Output</td>
<td>1.7</td>
<td>1.8</td>
<td>1.9</td>
<td></td>
</tr>
<tr>
<td>VREF</td>
<td>Input Reference Voltage</td>
<td>0.49 x VDDQ</td>
<td>0.50 x VDDQ</td>
<td>0.51 x VDDQ</td>
<td></td>
</tr>
<tr>
<td>VTT</td>
<td>Termination Voltage</td>
<td>VREF - 0.04</td>
<td>VREF</td>
<td>VREF + 0.04</td>
<td></td>
</tr>
</tbody>
</table>

19 CPU pins, 16 Mem I pins & 16 Mem II pins @ 20mA

Component Voltage (V)
- VDD
- GND

DC Resistance:
- 575mOhm
- 498mOhm
- 469mOhm
PDN Impedance of 1.8V Net

- 3 PDN Impedances are plotted from three different components:
  - D1 the memory controller
  - D3 and D4 the memory modules
Spatial Impedance Plot

Impedance plot on P1V8 plane seen from memory controller

Impedance plot on P1V8 plane seen from memory module I

Impedance plot on P1V8 plane seen from memory module II

@2.6GHz
Decap Placement

Decaps shifts the high impedance at its placement area
SSO Analysis for 2 DQ lines

- DDR2-400 I/O Buffer IBIS
- PRBS $N=7$
Transient Response

No Decaps

Power Supply VDD

With Decaps
Decap Analysis Tool

Over designing the PCB $\Rightarrow$ Additional BOM cost $\Rightarrow$ slightly or without performance improvement

Multiple goals:
- Optimizing the BOM cost
- Optimizing the PDN impedance

1. Define the target impedance
2. Define the list of parts for optimization
3. Start the optimization
Decap Analysis Tool Optimization (Step 1)

Target Impedance

Part lib. of current Decaps mounted on PCB
Decap Analysis Tool Optimization (Step 2)

Removing the decaps from PCB (Bare board)
Decap Analysis Tool - Results

Locate the marker to impedance curve manually and optimizing the impedance

Impedance curve with 10 decaps

Initial config. with 23 decaps

Before: 76¢
After : 52¢
Decap Analysis Tool - Results (II)

Run the automatic impedance optimization

Before: 76¢
After: 33¢
PDN Impedance: PCB + I/O Buffer Pckg

PDN Impedance Z

VDD Line

PACKAGE

PCB

VSS Line

VRM

<table>
<thead>
<tr>
<th>Pin</th>
<th>signal_name</th>
<th>model_name</th>
<th>R_pin</th>
<th>L_pin</th>
<th>C_pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>VDD</td>
<td>POWER</td>
<td>28.06m</td>
<td>0.83nH</td>
<td>0.12pF</td>
</tr>
<tr>
<td>A2</td>
<td>NC</td>
<td>NP_INPUT</td>
<td>35.40m</td>
<td>1.33nH</td>
<td>0.10pF</td>
</tr>
<tr>
<td>A3</td>
<td>VSS</td>
<td>GND</td>
<td>10.76m</td>
<td>0.23nH</td>
<td>NA</td>
</tr>
<tr>
<td>A7</td>
<td>VSSG</td>
<td>GND</td>
<td>17.01m</td>
<td>0.44nH</td>
<td>NA</td>
</tr>
<tr>
<td>A0</td>
<td>N0_DQS#</td>
<td>DQS#</td>
<td>45.74m</td>
<td>1.66nH</td>
<td>0.10pF</td>
</tr>
<tr>
<td>A9</td>
<td>VDDQ</td>
<td>POWER</td>
<td>1.94m</td>
<td>0.02nH</td>
<td>0.12pF</td>
</tr>
<tr>
<td>D1</td>
<td>MT</td>
<td>NP_INPUT</td>
<td>53.39m</td>
<td>1.95nH</td>
<td>0.14pF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>R_pkg</th>
<th>L_min</th>
<th>L_max</th>
<th>L_pkg</th>
<th>C_min</th>
<th>C_max</th>
</tr>
</thead>
<tbody>
<tr>
<td>36.92m</td>
<td>19.36m</td>
<td>76.39m</td>
<td>1.33nH</td>
<td>0.63nH</td>
<td>2.77nH</td>
</tr>
<tr>
<td>0.11pF</td>
<td>0.08pF</td>
<td>0.38pF</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
PDN Impedance Comparison

Series resistive and inductance from package
PDN Impedance: PCB + Package + Chip

- **SPICE model from Vendor**
- or
- using “c_comp” keyword from I/O buffer IBIS
PDN Impedance Comparison

Lumped RC DIE or better SPICE improve the high frequency PDN Imp.
SSO Analysis Setup

CHIP SPICE model

RLC Package
Transient Response

Max Noise: 1.89V
Max Noise: 1.84V
Impedance Measurement Method

Two port shunt-through measurement:
Measuring the $Z_{DUT}$

One port measurement:
Measuring the $Z_{connection} + Z_{DUT}$

\[
Z_{11} = \left. \frac{V_1}{I_1} \right|_{I_2=0} = Z_{connection} + Z_{DUT} \\
Z_{12} = \left. \frac{V_1}{I_2} \right|_{I_1=0} = \frac{V_2}{I_2} \cdot \frac{Z_{DUT}}{Z_{connection} + Z_{DUT}} = Z_{DUT}
\]
Probing Position

Goals:

- Very small layout area for probing (2mm²)
- High frequency measurement (up to 10GHz)
Comparison

Measurement of bareboard

Measurement with mounted decaps
Conclusions

Frequency Domain Analysis

• Quick and less computational effort
• Optimization via Decap Tool analysis
• No charging effect

Time Domain Analysis

• Provides more realistic I/O behavior (using IBIS buffer)
• Higher simulation time for complex board → HPC

Impedance Measurement

• One Port measurement
• Two port measurement